THE UNITED STATES PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

APPLICANT: M. A. Fathimulla et al. CASE NO.: P02,0004 01 (H0002270 DIV 1)

SERIAL NO.: 10/764,938 CONFIRMATION NO.: unknown

FILING DATE: January 26, 2004 GROUP ART UNIT: unknown

INVENTION: "SILICON-ON-INSULATOR WAFER FOR RF INTEGRATED CIRCUIT"

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

The patents and/or publication listed on the enclosed PTO Form-1449 are submitted pursuant to 37 CFR § § § 1.56, 1.97, and 1.98. Copies of the patents or publications noted on the Form-1449 are enclosed herewith. Also, a copy of an International Search Report is enclosed.

This Information Disclosure Statement is being filed, to the best of the undersigned's knowledge, before the mailing date of a first Office Action on the merits. Therefore, in accordance with 37 CFR §1.197(b), no certification or fee is required.

The Commissioner is hereby authorized to charge any additional fees that may be required, or to credit any overpayment, to account No. 501519.

An early and favorable action on the merits is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to:

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on April 28, 2004.

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Form PTO-1449	Docket No. P02,0004 01	Serial No. 10/764,938
INFORMATION DISCLOSURE CITATION IN AN APPLICATION (use several sheets if necessary)	Applicant Mohammed A. Fathimulla et al.	
	Filing Date 01/26/2004	Group Art Unit unknown

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate
	AA	5,168,078	12/01/92	Reisman et al.			
	AB	5,266,135	11/30/93	Short etal.			
	AC	5,362,667	11/8/94	Linn et al.			
	AD	5,387,555	02/07/95	Linn et al.			
	AE	5,569,620	10/29/96	Linn et al.			
	AF	5,728,624	03/17/98	Linn et al.			
	AG	5,801,084	09/01/98	Beasom et al.			
	AH	5,849,627	12/15/98	Linn et al.			
	AI	6,150,197	11/21/00	Boles et al.			
	AJ	6,183,857	02/06/01	Litwin et al.			
	AK	6,239,004	05/29/01	Aga et al.			
	AL	6,255,731	07/03/01	Ohmi et al.			
	AM	6,352,909	03/05/02	Usenko			
	AN	6,388,290	05/14/02	Celler et al.			
	AO	6,410,371	06/25/02	Yu et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AP							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AQ	Matsumoto et al., "A Novel High-speed Quasi-SOI Power MOSFET with Suppressed Parasitic Bipolar Effect Fabricated by Reversed Silicon Wafer Direct Bonding", IEDM 96- 1996, pp. 18.8.1 to 18.8.3.
	AR	Hisamoto et al., "Silicon RF Devices Fabricated by ULSI Processes Featuring 0.1-μm SOI-CMOS and Suspended Inductors", 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 104-105.
	AS	Matsumoto et al., "Study on the Devices Characteristics of a Quasi-SOI Power MOSFET Fabricated by Reversed Silicon Wafer Direct Bonding", 1998 IEEE, Vol. 45, pp. 1940-1945.
	AT	A.O. Adan et al., "SOI as a Mainstream IC Technology", Proceedings 1998 IEEE Intl. SOI Conference, Oct. 1998, pp. 9-12.
	AU	I. Lagnado et al., "RF Systems Based on Silicon-on-Sapphire Technology", 2000 IEEE Intl. SOI Conference, Oct. 2000, pp. 32-33.
	AV	Fiorenza et al., "RF Power LDMOSFET on SOI", IEEE Electron Device Letters, Vol. 22, March 2001, pp. 139-141.
	AW	

Examiner	Date Considered

***EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

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							Applicant Mohammed A. Fathimulla et al.	
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U.S. PATENT DOCUMENTS								
Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate	
	AA	6,291,324	09/18/01	Lescot et al.				
	AB	6,251,751	06/26/01	Chu et al.				
	AC	6,265,248	07/24/01	Darmawan et al.				
	AD	6,465,324	10/15/02	Vogt et al.				
	AE	5,773,355	06/30/98	Inoue et al.				
	AF	2002/0008268	01/24/02	Babcock et al.				
	AG	2002/0092307	07/18/02	Ghoshal				
	AH	5,920,764	07/06/99	Hanson et al.				
	AI	5,366,923	11/22/94	Beyer et al.				
	AJ							
	AK							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AL	EP 0 969 500 A2	01/05/00	European				
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AM	Matsumoto et al., "A High-Efficiency Thin-Film SOI Power MOSFET Having a Self-Aligned Offset Gate Structure for Multi-Gigahertz Applications", IEEE Transactions on Electron Devices, Vol. 48, No. 6, June 2001, pp. 1270-1274.						
	AN	Y. Hiraoka et al., "New substrate-crosstalk reduction structure using SOI substrate", 2001 IEEE Intl. SOI Conference, Oct. 2001, pp. 107-108.						
	AO	V. Cuocs et al., "A Novel Vertical DMOS Transistor in SOA Technology for RF-power Applications", Proc. 23rd Intl. Conference on Microelectronics, Vol 1, May 2002, pp. 159-162.						
	AP	A. O. Adan et al., "Linearity and Low-Noise Performance of SOI", IEEE Transactions on Electron Devices, Vol. 49, No. 5, May 2002, pp. 881-888.						
	AQ	Peter Van Zant, "Microchip Fabrication, A Practical Guide to Semiconductor Processing", Fourth Edition, McGraw-Hill, pp. 32-34.						
	AR							
	AS							
Examiner			Date Considered					

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